AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A programmable logic device (PLD) comprising:

a battery voltage pin;

a battery controller connected to the battery voltage pin; and

at least one critical circuit implemented in programmable logic of the PLD and selectively connected to the battery voltage pin,

a memory for storing a charging algorithm and a charging methodology associated with a battery connectable to the battery voltage pin;

a voltage source pin connected to the at least one critical circuit; and

a voltage detector connected to the voltage source pin, the voltage detector selectively connecting the battery voltage pin to the at least one critical circuit in response to a voltage drop at the voltage source pin.

2. (Original) The PLD of Claim 1, wherein the battery controller includes:

a battery charger controlled by the battery controller and operatively coupled to the battery voltage pin, the battery charger for charging the battery using the charging algorithm and the charging methodology.

3. (Cancelled)

4. (Original) The PLD of Claim 1, wherein the battery controller further includes end of life circuitry operatively coupled to the battery voltage pin.

5. (Original) The PLD of Claim 1, wherein the battery controller includes programmable logic resources.

Claims 6 and 7. (Cancelled)

8. (Currently Amended) ~~The PLD of Claim 7, further including:~~ A programmable logic device (PLD) comprising:

a first battery voltage pin;

a second battery voltage pin;

a battery controller selectively connected to one of the first battery voltage pin and the second battery voltage pin;

at least one critical circuit implemented in programmable logic of the PLD and selectively connected to one of the first battery voltage pin and the second battery voltage pin;

a voltage source pin connected to the at least one critical circuit;

a selector arrangement coupled to the first and second battery voltage pins and adapted to couple the at least one critical circuit to one of the first and second battery voltage pins;

an analog demultiplexer including an input terminal connected to the battery controller, a first output terminal selectively connected to the first battery voltage pin, and a second output terminal selectively connected to the second battery voltage pin; and

an analog multiplexer including a first input terminal connected to the first battery voltage pin, a second input terminal connected to the second battery voltage pin, and an output terminal selectively connected to the at least one critical circuit.

9. (Original) The PLD of Claim 8, wherein the battery controller includes:

a memory for storing a plurality of charging algorithms and a plurality of charging methodologies, wherein a first charging algorithm and a first charging methodology are associated with a first battery external to the PLD and connectable to the first battery voltage pin, and wherein a second charging algorithm and a second charging methodology are associated with a second battery external to the PLD and connectable to the second battery voltage pin; and

a battery charger controlled by the battery controller and operatively coupled to an input terminal of the analog demultiplexer, the battery charger for charging one of the first battery using the first charging algorithm and the first charging methodology and the second battery using the second charging algorithm and the second charging methodology.

10. (Previously Presented) The PLD of Claim 8, wherein the selector arrangement includes:

a voltage detector connected to the voltage source pin, the voltage detector selectively connecting the output terminal of the analog multiplexer to the at least one critical circuit.

11. (Original) The PLD of Claim 8, wherein the battery controller further includes end of life circuitry operatively coupled to at least one the first battery voltage pin and the second battery voltage pin.

12. (Currently Amended) The PLD of Claim [6] 8, wherein the battery controller includes programmable logic resources.

Claims 13-19. (Cancelled)

20. (Currently Amended) ~~The method of Claim 19, further including:~~ A method of fabricating a programmable logic device (PLD), the method comprising:

providing a first battery voltage pin;

providing a second battery voltage pin;

providing a selective connection between a battery controller and one of the first battery voltage pin and the second battery voltage pin;

providing a selective connection between programmable logic of the PLD and one of the first battery voltage pin and the second battery voltage pin;

providing a volatile memory for storing a plurality of charging algorithms and a plurality of charging methodologies, wherein a first charging algorithm and a first charging methodology are associated with a first battery connectable to the first battery voltage pin, and a second charging algorithm and a second charging methodology are associated with a second battery connectable to the second battery voltage pin;

connecting an input terminal of a demultiplexer to the battery controller;

providing a selective connection between a first output terminal of the demultiplexer and the first battery voltage pin;

providing a selective connection between a second output terminal of the demultiplexer and the second battery voltage pin;

connecting a first input terminal of a multiplexer to the first battery voltage pin;

connecting a second input terminal of the multiplexer to the second battery voltage pin; and

providing a selective connection between an output terminal of the multiplexer and the at least one critical circuit.

21. (Original) The method of Claim 20, further including:

coupling a battery charger, controlled by the battery controller, to the input terminal of the demultiplexer, the battery charger for charging one of the first battery using the first charging algorithm and the first charging methodology and the second battery using the second charging algorithm and the second charging methodology.

22. (Original) The method of Claim 21, further including:

connecting a voltage source pin to the at least one critical circuit; and

connecting a voltage detector to the voltage source pin, the voltage detector for selectively connecting the output terminal of the analog multiplexer to the at least one critical circuit.

23. (Original) The method of Claim 22, further including providing a selective connection between end of life circuitry and at least one of the first battery voltage pin and the second battery voltage pin.

24. (Currently Amended) The method of Claim [18] 20, further including implementing at least one of the selective connections with programmable logic resources.

Claims 25-31. (Cancelled)